AND8080/D

TSOP vs. SC70 Leadless Package Thermal Performance

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APPLICATION NOTE

Introduction

Leadless packages are becoming a popular method to reduce the size of a package while keeping the same silicon performance. This Application Note explores the differences between these two packaging methods to show the benefits of this promising new technology. The main advantages include:

- Improved thermal performance
- Reduced electrical parasitics
- Reduced size and mass of the package
- Improved board space efficiency

Construction Comparison

The main difference between these two package styles is the leads. The TSOP package has five leads that protrude outside the package whereas the Leadless package has only pads on the bottom of the package. Figure 2 illustrates the lead frame and external package differences.

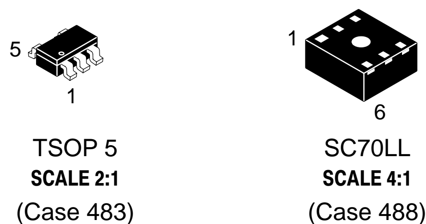

Figure 1. Profile comparison

The SC70LL has about a 45% smaller footprint than the TSOP5. Both packages can handle the same size of silicon device. The TSOP–5 package typically uses a eutectic gold die attach where as the SC70LL package requires a silver filled epoxy die attach.

Although wire lengths are approximately equal, the distance from the wire bond to the board traces is considerably longer in the TSOP–5. This adds to the electrical parasitics and can degrade package performance at high switching speeds.

Thermal Comparison

The Leadless package has a 20–25% lower thermal resistance than the TSOP package for steady state applications, as can be seen in Table 1. Again this is primarily due to the lead length out to the board traces. These packages were characterized on the same type of printed circuit board (PCB) with identical copper thickness for the traces, and each uses a 1.0 x 1.5 mm silicon die.

Table 1. Steady State Thermal Comparison

Metric	SC70LL	TSOP–5	
Theta JA (Note 1)	180	200	°C/W
Theta JA (Note 2)	115	150	°C/W
Psi JB (Note 2)	65	105	°C/W

1. Minimum copper pad configuration.
2. Package centered in a 1 inch copper pad.

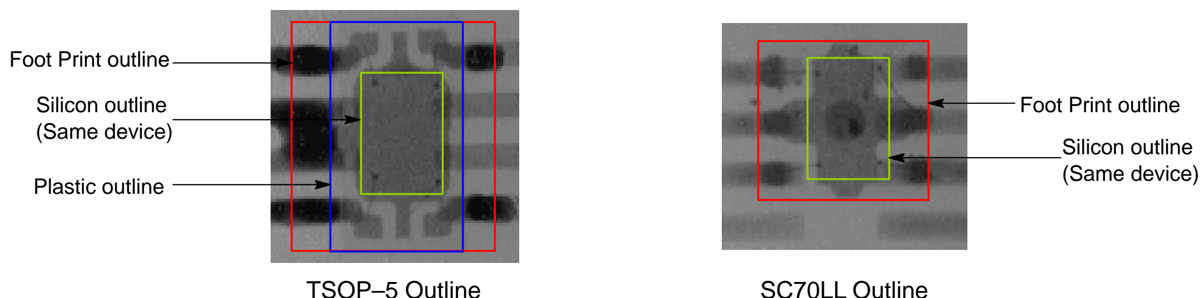

Figure 2. X–ray comparison of TSOP5 and SC70LL

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For applications where the transient thermal performance rules, the SC70LL package again out performs the TSOP–5 package as can be seen in the graph below (Figure 3).

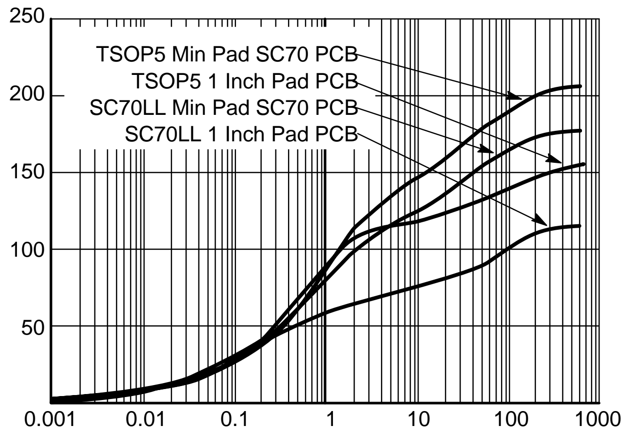


Figure 3. Single Pulse Transient thermal Performance (60 x 42 mil device)

The SC70LL package will allow the heat to get to the PCB much quicker than the TSOP package. The heat will get to the PCB in about 300 msec. for the SC70LL, but for the TSOP it will take over 2 seconds. before the heat gets to the PCB. This in turn will allow the package to respond to transient pulses faster and in some situations reduce the peak temperatures seen by the silicon.

A thermal SPICE model can be derived from the data in Figure 3 to represent the transient behavior of the packages. The result is shown in Table 2. An alternative is to use the equivalent mathematical thermal model shown in Table 3 based on a grounded thermal network. This can be implemented in spreadsheet tools by using the following relationship:

$$R(t) = \sum R_n \cdot (1 - e^{-t/\tau_n}) \quad (1)$$

Where: t, time [sec]
τ_n is the characteristic time [sec]
R_n is the ladder thermal resistance [°C/W]
R(t) is the transient resistance [°C/W]

Table 2. Thermal Spice Model of the SC70LL and the TSOP Package

SPICE Deck Format			SC70LL		TSOP5		Units
Node Name	Node1	Node2	Min pad	1 inch pad	Min pad	1 inch pad	
C_C1	GND	node_e	1.83261	3.43515	1.31102	3.86562	W–s/°C
C_C2	GND	node_d	0.306185	1.15654	0.239691	1.41822	W–s/°C
C_C3	GND	node_c	0.0202232	0.0812973	0.0173751	0.0355754	W–s/°C
C_C4	GND	node_b	0.00583821	0.00776804	0.00565366	0.00529866	W–s/°C
C_C5	GND	node_a	0.00096143	0.00096143	0.00096143	0.0010526	W–s/°C
C_C6	GND	d1	0.00019226	0.00019226	0.00019226	0.00019226	W–s/°C
R_R1	GND	node_e	34.2231	23.7248	34.9967	19.9024	°C/W
R_R2	node_e	node_d	34.2231	23.7248	34.9967	19.9024	°C/W
R_R3	node_d	node_c	38.3008	11.4839	40.2305	19.7158	°C/W
R_R4	node_c	node_b	46.7942	33.3159	91.4059	73.9007	°C/W
R_R5	node_b	node_a	20.9689	20.9689	20.9689	19.8619	°C/W
R_R6	node_a	d1	2.17062	2.17062	2.17062	2.17062	°C/W

Table 3. Thermal Model for Spreadsheet Estimation for the SC70LL and the TSOP Package

SC70LL/Min pad		SC70LL/1 inch pad		TSOP5/Min pad		TSOP5/1 inch pad	
R (°C/W)	tau (s)	R (°C/W)	tau (s)	R (°C/W)	tau (s)	R (°C/W)	tau (s)
1.49423	0.00034676	1.49424	0.00034676	1.56479	0.00035483	1.53957	0.00035193
14.5764	0.0199923	15.9177	0.0208857	11.1228	0.0177874	13.1191	0.0198708
22.7674	0.222669	28.5038	0.260653	24.0824	0.256978	34.2969	0.354756
59.9204	1.04965	19.7816	0.996187	76.7849	1.12284	64.7652	0.937145
30.2724	9.4814	11.1735	20.0248	31.8987	9.48588	9.08486	19.3353
47.6499	76.1575	38.518	120.711	49.2099	76.1405	32.6482	115.755

Mounting Considerations

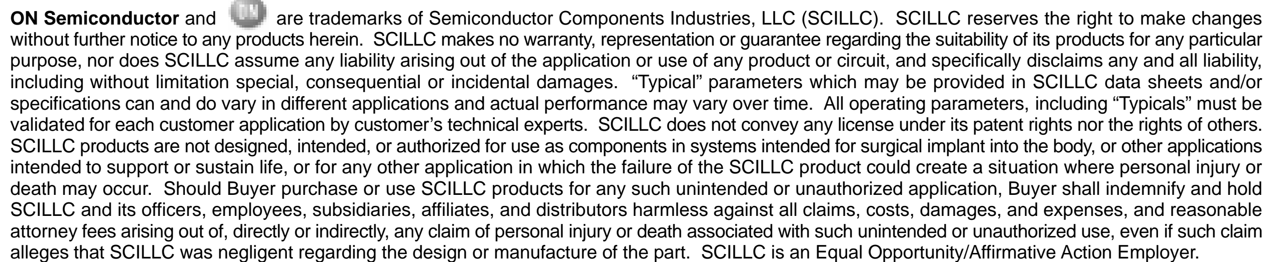
The thermal performance of a package is to a large degree a function of the thermal properties of the circuit board on which it is mounted. As can be seen in Table 1, the difference between a package mounted on a min pad PCB and a 1 inch pad PCB can be up to a 35% improvement in the steady state thermal performance.

In reality, the 1 inch pad PCB design is unrealistic since most of the applications using this package can not afford that amount of board space. Actual performance will likely be somewhere in between these extremes. Careful PCB design can optimize the thermal performance to get the most out of these packages.

In any case, the SC70LL package will thermally outperform the TSOP package in any mounting application, due to its close coupling to the PCB, especially if the exposed pad is connected to some copper area that will extend its thermal spreading capability.

Board mounting problems related to large copper areas may be avoided by judicious use of solder mask over the copper. (Note that this will not adversely affect the heat dissipating properties of the spreader area.)

Devices such as the NCP500, are manufactured in both the SC70LL and the TSOP–5 package. In thermally sensitive applications, it should be clear that the use of the Leadless package may provide a real advantage over the traditional package.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